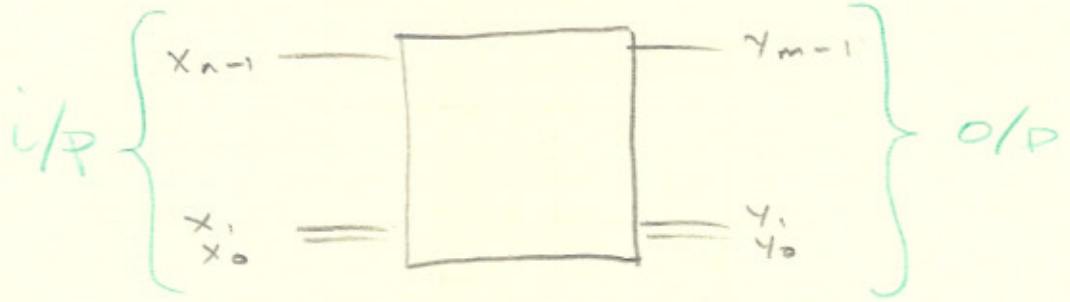
Coole Converters

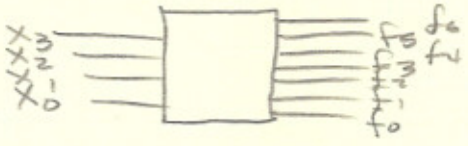


f_6

f_5 | f_7 | f_1

f_4 | | f_2

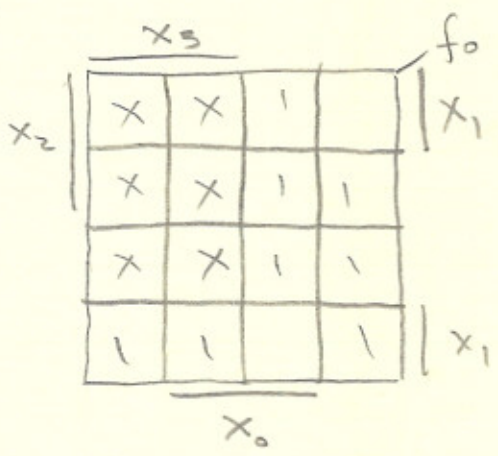
f_3



1//

x_3	x_2	x_1	x_0	f_0	f_1	f_2	f_3	f_4	f_5	f_6
0	0	0	0	0	1	1	1	1	1	1
0	0	0	1	0	0	0	0	1	1	0
0	0	1	0	1	0	1	1	0	1	1
0	0	1	1	1	0	0	1	1	1	1
0	1	0	0	1	1	0	0	1	1	0
0	1	0	1	1	1	0	1	1	0	1
0	1	1	0	1	1	1	1	1	0	1
0	1	1	1	0	0	0	0	1	1	1
1	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	1	0	1	1	1	1

2//



3//

$$f_0 = x_3 + x_1 + x_2 x_0 + \bar{x}_2 \cdot \bar{x}_0$$

Continue with other 6 carnal maps. to come up with logic circuits.

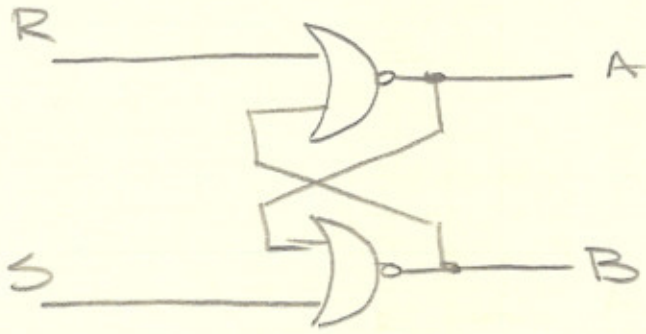
4// Design complex CMOS circuit.

5// VL simulation

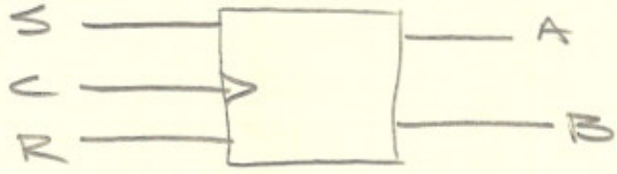
Latches

SR Latch

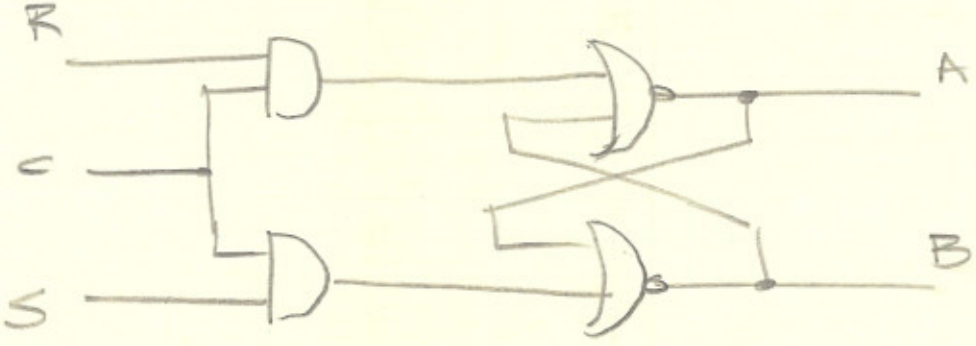
S	R	A_{t+1}	B_{t+1}
0	0	A_t	B_t
0	1	0	1
1	0	1	0
1	1	0	0

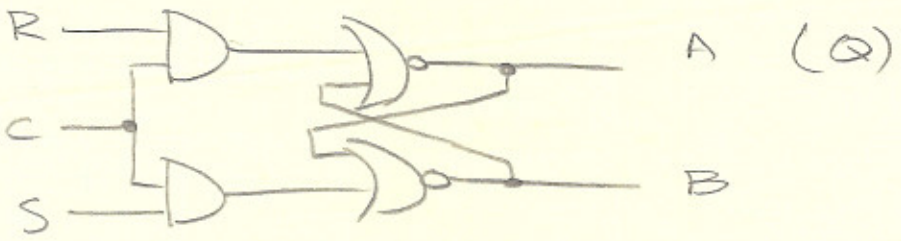


Gated SR latch

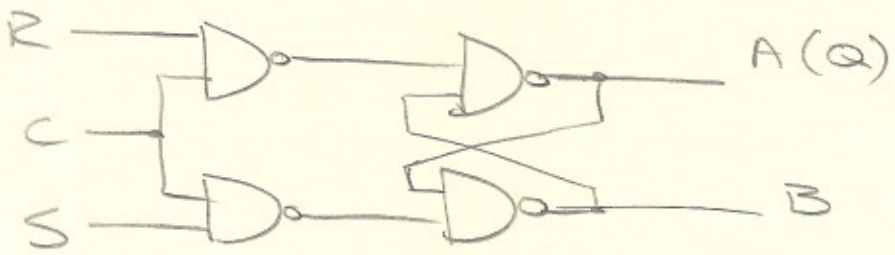


S	R	A_{t+1}	B_{t+1}
0	0	A_t	B_t
0	1	0	1
1	0	1	0
1	1	X	X

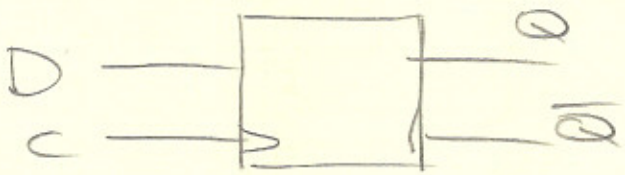




or



D Latch



D	Q_{t+1}
0	0
1	1